Your search matched **44** of **740919** documents.
Results are shown **25** to a page, sorted by **publication year** in **descending** order.
You may refine your search by editing the current search expression or entering a new one the text box.
Then click **Search Again**

register* <and> bypass* Search Again

Results:
Journal or Magazine = **JNL** Conference = **CNF** Standard = **STD**

1 **A contention-free mobility management scheme based on probabilistic paging**
Yuen, W.H.A.; Wing Shing Wong
Vehicular Technology, IEEE Transactions on , Volume: 50 Issue: 1 , Jan. 2001
Page(s): 48 -58

[Abstract] [PDF Full-Text (200 KB)] **JNL**

2 **Exploiting data forwarding to reduce the power budget of VLIW embedded processors**
Sami, M.; Sciuto, D.; Silvano, C.; Zaccaria, V.; Zafalom, R.
Design, Automation and Test in Europe, 2001. Conference and Exhibition 2001. Proceedings , 2001
Page(s): 252 -257

[Abstract] [PDF Full-Text (552 KB)] **CNF**

3 **A reconfigurable pipelined IDCT for low-energy video processing**
Suhwan Kim; Ziesler, C.H.; Papaefthymiou, M.C.
ASIC/SOC Conference, 2000. Proceedings. 13th Annual IEEE International , 2000
Page(s): 13 -17

[Abstract] [PDF Full-Text (416 KB)] **CNF**

4 **Cross-sectional area changes in peripheral vein grafts monitored by three-dimensional ultrasound imaging**
Leotta, D.F.; Primozich, J.F.; Beach, K.W.; Bergelin, R.O.; Gibson, K.D.; Strandness, D.E., Jr.
Ultrasonics Symposium, 2000 IEEE , Volume: 2 , 2000
Page(s): 1865 -1868 vol.2

[Abstract] [PDF Full-Text (336 KB)] **CNF**

5 **Register integration: a simple and efficient implementation of squash reuse**
Roth, A.; Sohi, G.S.
Microarchitecture, 2000. MICRO-33. Proceedings. 33rd Annual IEEE/ACM International Symposium on , 2000
Page(s): 223 -234

[Abstract] [PDF Full-Text (1232 KB)] CNF

6 **Multi-modality model-based registration in the cardiac domain**
O'Donnell, T.; Aharon, S.; Halliburton, S.S.; Gupta, A.; Funka-Lea, G.; White, R.D.
Computer Vision and Pattern Recognition, 2000. Proceedings. IEEE Conference on , Volume: 2 , 2000
Page(s): 790 -791 vol.2

[Abstract] [PDF Full-Text (168 KB)] CNF

7 **Energy-efficient register access**
Tseng, J.H.; Asanovic, K.
Integrated Circuits and Systems Design, 2000. Proceedings. 13th Symposium on , 2000
Page(s): 377 -382

[Abstract] [PDF Full-Text (468 KB)] CNF

8 **Multiple-banked register file architectures**
Cruz, J.-L.; Gonzalez, A.; Valero, M.; Topham, N.P.
Computer Architecture, 2000. Proceedings of the 27th International Symposium on , 2000
Page(s): 316 -325

[Abstract] [PDF Full-Text (800 KB)] CNF

9 **A 2.5-GFLOPS, 6.5 million polygons per second, four-way VLIW geometry processor with SIMD instructions and a software bypass mechanism**
Kubosawa, H.; Higaki, N.; Ando, S.; Takahashi, H.; Asada, Y.; Anbutsu, H.; Sato, T.; Sakate, M.; Suga, A.; Kimura, M.; Miyake, H.; Okano, H.; Asato, A.; Kimura, Y.; Nakayama, H.; Kimoto, M.; Hirochi, K.; Saito, H.; Kaido, N.; Nakagawa, Y.; Shimada, T.
Solid-State Circuits, IEEE Journal of , Volume: 34 Issue: 11 , Nov. 1999
Page(s): 1619 -1626

[Abstract] [PDF Full-Text (1000 KB)] JNL

10 **Fast and fair mutual exclusion for shared memory systems**
Ting-Lu Huang
Distributed Computing Systems, 1999. Proceedings. 19th IEEE International Conference on , 1999
Page(s): 224 -231

[Abstract] [PDF Full-Text (240 KB)] CNF

11 **A 500 MHz, write-bypassed, 88-entry, 90-bit register file**
Golden, M.; Partovi, H.
VLSI Circuits, 1999. Digest of Technical Papers. 1999 Symposium on , 1999
Page(s): 105 -108

[Abstract] [PDF Full-Text (288 KB)] CNF

12 **Interconnect-limited VLSI architecture**
Dally, W.J.
Interconnect Technology, 1999. IEEE International Conference , 1999
Page(s): 15 -17

[Abstract] [PDF Full-Text (284 KB)] CNF

13 **A 2.5 GFLOPS 6.5 million polygons per second 4-way VLIW geometry processor with SIMD instructions and a software bypass mechanism**
Higaki, N.; Kubosawa, H.; Ando, S.; Takahashi, H.; Asada, Y.; Anbutsu, H.; Sato, T.; Sakate, M.; Suga, A.; Kimura, M.; Miyake, H.; Okano, H.; Asato, A.; Kimura, Y.; Nakayama, H.; Kimoto, M.; Hirochi, K.; Saito, H.; Kaido, N.; Nakagawa, Y.; Shimada, T.
Solid-State Circuits Conference, 1999. Digest of Technical Papers. ISSCC. 1999 IEEE International , 1999
Page(s): 260 -261

[Abstract] [PDF Full-Text (300 KB)] CNF

14 **A 690 ps read-access latency register file for a GHz integer microprocessor**
Takahashi, O.; Silberman, J.; Dhong, S.; Hofstee, P.; Aoki, N.
Computer Design: VLSI in Computers and Processors, 1998. ICCD '98. Proceedings. International Conference on , 1998
Page(s): 6 -10

[Abstract] [PDF Full-Text (820 KB)] CNF

15 **Using precomputation in architecture and logic resynthesis**
Hassoun, S.; Ebeling, C.
Computer-Aided Design, 1998. ICCAD 98. Digest of Technical Papers. 1998 IEEE/ACM International Conference on , 1998
Page(s): 316 -323

[Abstract] [PDF Full-Text (748 KB)] CNF

16 **An x86 load/store unit with aggressive scheduling of load/store operations**
Hui-Yue Hwang; R-Ming Shiu; Jyh-Jiun Shann
Parallel and Distributed Systems, 1998. Proceedings. 1998 International Conference on , 1998
Page(s): 496 -503

[Abstract] [PDF Full-Text (140 KB)] CNF

17 **Compiler-directed early load-address generation**
Ben Chung Cheng; Connors, D.A.; Hwu, W.W.
Microarchitecture, 1998. MICRO-31. Proceedings. 31st Annual ACM/IEEE International Symposium on , 1998
Page(s): 138 -147

[Abstract] [PDF Full-Text (240 KB)] CNF

18 **Putting the fill unit to work: dynamic optimizations for trace cache microprocessors**
Friendly, D.H.; Patel, S.J.; Patt, Y.N.
Microarchitecture, 1998. MICRO-31. Proceedings. 31st Annual ACM/IEEE International Symposium

on , 1998
Page(s): 173 -181

[Abstract] [PDF Full-Text (96 KB)] CNF

19 **Effective cluster assignment for modulo scheduling**
Nystrom, E.; Eichenberger, A.E.
Microarchitecture, 1998. MICRO-31. Proceedings. 31st Annual ACM/IEEE International Symposium on , 1998
Page(s): 103 -114

[Abstract] [PDF Full-Text (128 KB)] CNF

20 **Reducing overheads of local communications in fine-grain parallel computation**
Jin-Soo Kim; Soonhoi Ha; Chu Shik Jhon
Parallel Processing, 1997., Proceedings of the 1997 International Conference on , 1997
Page(s): 223 -226

[Abstract] [PDF Full-Text (376 KB)] CNF

21 **Power reduction techniques for a spread spectrum based correlator**
Garrett, D.; Stan, M.
Low Power Electronics and Design, 1997. Proceedings., 1997 International Symposium on , 1997
Page(s): 225 -230

[Abstract] [PDF Full-Text (508 KB)] CNF

22 **An early-completion-detecting ALU for a 1 GHz 64 b datapath**
Kondo, Y.; Ikumi, N.; Ueno, K.; Mori, J.; Hirano, M.
Solid-State Circuits Conference, 1997. Digest of Technical Papers. 43rd ISSCC., 1997 IEEE International , 1997
Page(s): 418 -419, 497

[Abstract] [PDF Full-Text (1004 KB)] CNF

23 **Clock-powered logic for a 50 MHz low-power RISC datapath**
Tzartzanis, N.; Athas, W.C.
Solid-State Circuits Conference, 1997. Digest of Technical Papers. 43rd ISSCC., 1997 IEEE International , 1997
Page(s): 338 -339, 482

[Abstract] [PDF Full-Text (1192 KB)] CNF

24 **Architecture and performance of the Hitachi SR2201 massively parallel processor system**
Fujii, H.; Yasuda, Y.; Akashi, H.; Inagami, Y.; Koga, M.; Ishihara, O.; Kashiyama, M.; Wada, H.; Sumimoto, T.
Parallel Processing Symposium, 1997. Proceedings., 11th International , 1997
Page(s): 233 -241

[Abstract] [PDF Full-Text (836 KB)] CNF

25 **Autocircuit: a clock edge general behavioral synthesis system with a direct path to physical datapaths**
Ugurdag, H.F.; Fuhrman, T.E.
Computer Design: VLSI in Computers and Processors, 1996. ICCD '96. Proceedings., 1996 IEEE International Conference on , 1996
Page(s): 514 -523

[Abstract] [PDF Full-Text (1072 KB)] CNF

1 2 [Next]

Home | Log-out | Journals | Conference Proceedings | Standards | Search by Author | Basic Search | Advanced Search
Join IEEE | Web Account | New this week | OPAC Linking Information | Your Feedback | Email Alerting
No Robots Please | Release Notes | IEEE Online Publications | Help | FAQ| Terms | Back to Top

Your search matched **44** of **740919** documents.
Results are shown **25** to a page, sorted by **publication yearin descending**order.
You may refine your search by editing the current search expression or entering a new one the text box.
Then click **Search Again**

register* <and> bypass* Search Again

Results:
Journal or Magazine = **JNL** Conference = **CNF** Standard = **STD**

26 **CPU core generation for hardware-software codesign**
Kyung-Sik Jang; Kunieda, H.
Circuits and Systems, 1996., IEEE Asia Pacific Conference on , 1996
Page(s): 306 -309

[Abstract] [PDF Full-Text (400 KB)] **CNF**

27 **Reconfiguration techniques for a single scan chain**
Narayanan, S.; Breuer, M.A.
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 14 Issue: 6 , June 1995
Page(s): 750 -765

[Abstract] [PDF Full-Text (1676 KB)] **JNL**

28 **Caching processor general registers**
Yung, R.; Wilhelm, N.C.
Computer Design: VLSI in Computers and Processors, 1995. ICCD '95. Proceedings., 1995 IEEE International Conference on , 1995
Page(s): 307 -312

[Abstract] [PDF Full-Text (616 KB)] **CNF**

29 **The performance impact of incomplete bypassing in processor pipelines**
Ahuja, P.S.; Clark, D.W.; Rogers, A.
Microarchitecture, 1995., Proceedings of the 28th Annual International Symposium on , 1995
Page(s): 36 -45

[Abstract] [PDF Full-Text (992 KB)] **CNF**

30 **Improving CISC instruction decoding performance using a fill unit**
Smotherman, M.; Franklin, M.
Microarchitecture, 1995., Proceedings of the 28th Annual International Symposium on , 1995
Page(s): 219 -229

[Abstract] [PDF Full-Text (848 KB)] CNF

31 **A method for pseudo-exhaustive test pattern generation**
Kagaris, D.; Makedon, F.; Tragoudas, S.
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 13 Issue: 9 , Sept. 1994
Page(s): 1170 -1178

[Abstract] [PDF Full-Text (768 KB)] JNL

32 **Architectural verification of processors using symbolic instruction graphs**
Chandra, A.K.; Iyengar, V.S.; Jawalekar, R.V.; Mullen, M.P.; Nair, I.; Rosen, B.K.
Computer Design: VLSI in Computers and Processors, 1994. ICCD '94. Proceedings., IEEE International Conference on , 1994
Page(s): 454 -459

[Abstract] [PDF Full-Text (460 KB)] CNF

33 **Reconfigurable scan chains: A novel approach to reduce test application time**
Narayanan, S.; Breuer, M.A.
Computer-Aided Design, 1993. ICCAD-93. Digest of Technical Papers., 1993 IEEE/ACM International Conference on , 1993
Page(s): 710 -715

[Abstract] [PDF Full-Text (660 KB)] CNF

34 **Cache memories for data flow machines**
Takesue, M.
Computers, IEEE Transactions on , Volume: 41 Issue: 6 , June 1992
Page(s): 677 -687

[Abstract] [PDF Full-Text (952 KB)] JNL

35 **A metric towards efficient pseudo-exhaustive test pattern generation**
Kagaris, D.; Makedon, F.; Tragoudas, S.
Circuits and Systems, 1992. ISCAS '92. Proceedings., 1992 IEEE International Symposium on , Volume: 1 , 1992
Page(s): 379 -382 vol.1

[Abstract] [PDF Full-Text (348 KB)] CNF

36 **HARP: a VLIW RISC processor**
Findlay, P.A.; Trainis, S.A.; Steven, G.B.; Adams, R.G.
CompEuro '91. Advanced Computer Technology, Reliable Systems and Applications. 5th Annual European Computer Conference. Proceedings. , 1991
Page(s): 368 -372

[Abstract] [PDF Full-Text (364 KB)] CNF

37 **Evaluation of defect-tolerance scheme in a 600 M-bit wafer-scale memory**
Yamashita, K.; Ikehara, S.; Nagashima, M.; Tatematsu, T.
Wafer Scale Integration, 1991. Proceedings., [3rd] International Conference on , 1991
Page(s): 12 -18

[Abstract] [PDF Full-Text (264 KB)] **CNF**

38 **Quantification of retinal damage during cardiopulmonary bypass: comparison of computer and human assessment**
Jagoe, J.R.; Blauth, C.I.; Smith, P.L.; Arnold, J.V.; Taylor, K.M.; Wootton, R.
Communications, Speech and Vision, IEE Proceedings I [see also IEE Proceedings-Communications] , Volume: 137 Issue: 3 , June 1990
Page(s): 170 -175

[Abstract] [PDF Full-Text (1256 KB)] **JNL**

39 **Ultrafast all-optical switches in fiber networks**
Islam, M.N.; Sauer, J.R.
Optical Multiple Access Networks, 1990. Conference Digest. LEOS Summer Topical on , 1990
Page(s): 37 -38

[Abstract] [PDF Full-Text (104 KB)] **CNF**

40 **Performance comparison of load/store and symmetric instruction set architectures**
Alpert, D.; Averbuch, A.; Danieli, O.
Computer Architecture, 1990. Proceedings., 17th Annual International Symposium on , 1990
Page(s): 172 -181

[Abstract] [PDF Full-Text (624 KB)] **CNF**

41 **Self-testing and self-reconfiguration architecture for 2-D WSI arrays**
Abujbara, H.Y.; Al-Arian, S.A.
Parallel and Distributed Processing, 1990. Proceedings of the Second IEEE Symposium on , 1990
Page(s): 527 -530

[Abstract] [PDF Full-Text (320 KB)] **CNF**

42 **Soft-programmable bypass switch design for defect-tolerant arrays**
Walker, D.M.H.
Wafer Scale Integration, 1990. Proceedings., [2nd] International Conference on , 1990
Page(s): 236 -242

[Abstract] [PDF Full-Text (376 KB)] **CNF**

43 **Algorithms and architectures for concurrent Viterbi decoding**
Lin, H.-D.; Messerschmitt, D.G.
Communications, 1989. ICC '89, BOSTONICC/89. Conference record. 'World Prosperity Through Communications', IEEE International Conference on , 1989
Page(s): 836 -840 vol.2

[Abstract] [PDF Full-Text (468 KB)] CNF

44 **Computer Support Of Cardiovascular Surgical Registries**
Covvey, H.D.; MacGregor, D.C.; Smardon, S.; Wigle, E.D.
Computer Application in Medical Care, 1978. Proceedings. The Second Annual Symposium on
Page(s): 536 -544

[Abstract] [PDF Full-Text (504 KB)] CNF

[Prev] 1 2

Home | Log-out | Journals | Conference Proceedings | Standards | Search by Author | Basic Search | Advanced Search
Join IEEE | Web Account | New this week | OPAC Linking Information | Your Feedback | Email Alerting
No Robots Please | Release Notes | IEEE Online Publications | Help | FAQ| Terms | Back to Top

Welcome to IEEE Xplore

- Home
- Log-out

Tables of Contents

- Journals & Magazines
- Conference Proceedings
- Standards

Search

- By Author
- Basic
- Advanced

Member Services

- Join IEEE
- Establish IEEE Web Account

Your search matched **44** of **740919** documents.
Results are shown **25** to a page, sorted by **publication year** in **descending** order.
You may refine your search by editing the current search expression or entering a new one the text box.
Then click **Search Again**

register* <and> bypass* Search Again

Results:
Journal or Magazine = **JNL** Conference = **CNF** Standard = **STD**

26 **CPU core generation for hardware-software codesign**
Kyung-Sik Jang; Kunieda, H.
Circuits and Systems, 1996., IEEE Asia Pacific Conference on , 1996
Page(s): 306 -309

[Abstract] [PDF Full-Text (400 KB)] **CNF**

27 **Reconfiguration techniques for a single scan chain**
Narayanan, S.; Breuer, M.A.
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 14 Issue: 6 , June 1995
Page(s): 750 -765

[Abstract] [PDF Full-Text (1676 KB)] **JNL**

28 **Caching processor general registers**
Yung, R.; Wilhelm, N.C.
Computer Design: VLSI in Computers and Processors, 1995. ICCD '95. Proceedings., 1995 IEEE International Conference on , 1995
Page(s): 307 -312

[Abstract] [PDF Full-Text (616 KB)] **CNF**

29 **The performance impact of incomplete bypassing in processor pipelines**
Ahuja, P.S.; Clark, D.W.; Rogers, A.
Microarchitecture, 1995., Proceedings of the 28th Annual International Symposium on , 1995
Page(s): 36 -45

[Abstract] [PDF Full-Text (992 KB)] **CNF**

30 **Improving CISC instruction decoding performance using a fill unit**
Smotherman, M.; Franklin, M.
Microarchitecture, 1995., Proceedings of the 28th Annual International Symposium on , 1995
Page(s): 219 -229

[Abstract] [PDF Full-Text (848 KB)] CNF

31 **A method for pseudo-exhaustive test pattern generation**
Kagaris, D.; Makedon, F.; Tragoudas, S.
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 13 Issue: 9 , Sept. 1994
Page(s): 1170 -1178

[Abstract] [PDF Full-Text (768 KB)] JNL

32 **Architectural verification of processors using symbolic instruction graphs**
Chandra, A.K.; Iyengar, V.S.; Jawalekar, R.V.; Mullen, M.P.; Nair, I.; Rosen, B.K.
Computer Design: VLSI in Computers and Processors, 1994. ICCD '94. Proceedings., IEEE International Conference on , 1994
Page(s): 454 -459

[Abstract] [PDF Full-Text (460 KB)] CNF

33 **Reconfigurable scan chains: A novel approach to reduce test application time**
Narayanan, S.; Breuer, M.A.
Computer-Aided Design, 1993. ICCAD-93. Digest of Technical Papers., 1993 IEEE/ACM International Conference on , 1993
Page(s): 710 -715

[Abstract] [PDF Full-Text (660 KB)] CNF

34 **Cache memories for data flow machines**
Takesue, M.
Computers, IEEE Transactions on , Volume: 41 Issue: 6 , June 1992
Page(s): 677 -687

[Abstract] [PDF Full-Text (952 KB)] JNL

35 **A metric towards efficient pseudo-exhaustive test pattern generation**
Kagaris, D.; Makedon, F.; Tragoudas, S.
Circuits and Systems, 1992. ISCAS '92. Proceedings., 1992 IEEE International Symposium on , Volume: 1 , 1992
Page(s): 379 -382 vol.1

[Abstract] [PDF Full-Text (348 KB)] CNF

36 **HARP: a VLIW RISC processor**
Findlay, P.A.; Trainis, S.A.; Steven, G.B.; Adams, R.G.
CompEuro '91. Advanced Computer Technology, Reliable Systems and Applications. 5th Annual European Computer Conference. Proceedings. , 1991
Page(s): 368 -372

[Abstract] [PDF Full-Text (364 KB)] CNF

37 **Evaluation of defect-tolerance scheme in a 600 M-bit wafer-scale memory**
Yamashita, K.; Ikehara, S.; Nagashima, M.; Tatematsu, T.
Wafer Scale Integration, 1991. Proceedings., [3rd] International Conference on , 1991
Page(s): 12 -18

[Abstract] [PDF Full-Text (264 KB)] CNF

38 **Quantification of retinal damage during cardiopulmonary bypass: comparison of computer and human assessment**
Jagoe, J.R.; Blauth, C.I.; Smith, P.L.; Arnold, J.V.; Taylor, K.M.; Wootton, R.
Communications, Speech and Vision, IEE Proceedings I [see also IEE Proceedings-Communications] , Volume: 137 Issue: 3 , June 1990
Page(s): 170 -175

[Abstract] [PDF Full-Text (1256 KB)] JNL

39 **Ultrafast all-optical switches in fiber networks**
Islam, M.N.; Sauer, J.R.
Optical Multiple Access Networks, 1990. Conference Digest. LEOS Summer Topical on , 1990
Page(s): 37 -38

[Abstract] [PDF Full-Text (104 KB)] CNF

40 **Performance comparison of load/store and symmetric instruction set architectures**
Alpert, D.; Averbuch, A.; Danieli, O.
Computer Architecture, 1990. Proceedings., 17th Annual International Symposium on , 1990
Page(s): 172 -181

[Abstract] [PDF Full-Text (624 KB)] CNF

41 **Self-testing and self-reconfiguration architecture for 2-D WSI arrays**
Abujbara, H.Y.; Al-Arian, S.A.
Parallel and Distributed Processing, 1990. Proceedings of the Second IEEE Symposium on , 1990
Page(s): 527 -530

[Abstract] [PDF Full-Text (320 KB)] CNF

42 **Soft-programmable bypass switch design for defect-tolerant arrays**
Walker, D.M.H.
Wafer Scale Integration, 1990. Proceedings., [2nd] International Conference on , 1990
Page(s): 236 -242

[Abstract] [PDF Full-Text (376 KB)] CNF

43 **Algorithms and architectures for concurrent Viterbi decoding**
Lin, H.-D.; Messerschmitt, D.G.
Communications, 1989. ICC '89, BOSTONICC/89. Conference record. 'World Prosperity Through Communications', IEEE International Conference on , 1989
Page(s): 836 -840 vol.2

[Abstract] [PDF Full-Text (468 KB)] CNF

44 **Computer Support Of Cardiovascular Surgical Registries**
Covvey, H.D.; MacGregor, D.C.; Smardon, S.; Wigle, E.D.
Computer Application in Medical Care, 1978. Proceedings. The Second Annual Symposium on
Page(s): 536 -544

[Abstract] [PDF Full-Text (504 KB)] CNF

[Prev] 1 2

Home | Log-out | Journals | Conference Proceedings | Standards | Search by Author | Basic Search | Advanced Search
Join IEEE | Web Account | New this week | OPAC Linking Information | Your Feedback | Email Alerting
No Robots Please | Release Notes | IEEE Online Publications | Help | FAQ| Terms | Back to Top